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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,887	10/19/1999	PUTHIYA K. NIZAR	042390.P7149	3400

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EXAMINER
TRAN, DENISE

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/420,887	NIZAR ET AL.	
	Examiner	Art Unit	
	Denise Tran	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-23 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ryan US 2001/0042163 A1.

As per claims 1, 13 and 17, Ryan teaches the use of a memory translation hub comprising:

a memory channel interface that receives a memory control packet from a memory channel (e.g. figure 4 and abstract);

a memory bus interface that provides a memory bus (e.g. fig. 4 and abstract); and

a command generator coupled to the memory channel interface and to the memory bus interface, the command generator causing the memory bus interface to provide memory control signals on the memory bus responsive to the memory control packet (e.g. fig. 4 and abstract).

As per claims 2 and 14, Ryan teaches the use of the memory channel includes a control portion an a data portion, the memory channel interface receiving a memory control packet only from the control portion of the memory channel (e.g. fig. 4, els. 8 and 16).

As per claim 3, Ryan teaches the use of the memory control packet includes command flag bits that indicate that the memory control packet is one of an activate command, a read/write command, and an extended command (e.g. fig. 4, abstract and paragraph 29).

As per claim 4, Ryan teaches the use of the memory control packet specifies a memory row, a memory row address, a memory bank address and a device identification mask if the memory control packet is the activate command (e.g. figs. 3-4, and signals on el. 154 of fig. 4).

As per claim 5, Ryan teaches the use of the memory control packet specifies a memory row, a memory column address, and a memory bank address, if the memory control packet is the read/write command (e.g. figs. 3-4, and signals on el. 154 of fig. 4).

As per claim 6, Ryan teaches the use of if the memory control packet is the extended command, the memory control packet includes extended flag bits that indicate that the memory control packet is one of a retire with mask command, a pre-charge command, and a service command (e.g. paragraphs 29 and 32-36).

As per claim 7, Ryan teaches the use of the memory control packet specifies a memory row, and a byte mask, if the memory control packet is the retire and mask command (e.g. paragraphs 33-35).

As per claim 8, Ryan teaches the use of the memory control packet specifies a memory row, and one of a broadcast flag and a memory bank address, if the memory control packet is the precharge command (e.g. paragraph 32).

As per claim 9, Ryan teaches the use of the memory control packet specifies a memory row, an operation, and one of a broadcast flag and a memory bank address, if the memory control packet is the service command (e.g. paragraphs 29-35).

As per claim 10, the use of refresh commands is an inherent feature of Ryan. Refreshing allows the data within the RAM to be maintained (i.e., prevent from being lost).

As per claims 11, 15 and 18, Ryan teaches the use of a write logic circuit coupled to the memory channel interface and to the memory us interface, the write logic circuit receiving a write data packet from the memory channel interface and causing the memory bus interface to provide memory control signals and data signals on the memory bus responsive to the write data packet, the memory channel interface receiving a write data packet only from the data portion of the memory channel (e.g. fig. 4, els. 140, 146, 158, 150, 152, 160).

As per claims 12, 16 and 19, Ryan teaches the use of a read logic circuit coupled to the memory channel interface and to the memory bus interface, the read logic circuit receiving read data from the memory bus interface, generating a read data packet containing the read data, and causing the memory channel interface to transmit the read data packet on the data portion of the memory channel (e.g. fig. 4, els. 140, 146, 158, 150, 152, 162).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nizar et al., U.S. Patent No. 6,378,056, hereinafter Nizar in view of Ryan, US 2001/0042163 A1.

As per claim 20, Nizar shows the use of a memory subsystem comprising:

a memory control hub (e.g. fig.5, el. 500);

a memory channel coupled to the memory control hub (e.g. fig. 5, els. 540 and 530).

Nizar does not specifically show the use of a memory bus, a memory device coupled to the memory bus, and a memory translation hub coupled to the memory channel and to the memory bus, the memory translation hub to receive a memory control packet from the memory channel, and to generate memory control signals on the memory bus responsive to the memory control packet. Ryan shows the use of a memory bus, a memory device coupled to the memory bus, and a memory translation hub coupled to the memory channel and to the memory bus, the memory translation hub to receive a memory control packet from the memory channel, and to generate memory control signals on the memory bus responsive to the memory control packet (e.g. figure 4 and abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ryan with Nizar because it would provide for different types of memory devices to be compatible with existing systems.

As per claim 21, Ryan shows the use of the memory channel includes a control portion and data portion, the memory translation hub receiving a memory control packet only from the control portion of the memory channel (e.g. fig. 4, els. 8 and 16).). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ryan with Nizar because it would provide for different types of memory devices to be compatible with existing systems.

As per claim 22, Ryan shows the use of the memory translation hub further receives a write data packet from the data portion of the memory channel, and generates memory control signals and data signals on the memory bus responsive to the write data packet (e.g. fig. 4, els. 140, 146, 158, 150, 152, 160). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ryan with Nizar because it would provide for different types of memory devices to be compatible with existing systems.

As per claim 23, Ryan shows the use of the memory translation hub further receives read data from the memory bus interface, generates a read data packet containing the read data, and transmits the read data packet on the data portion of the memory channel (e.g. fig. 4, els. 140, 146, 158, 150, 152, 162). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine

Ryan with Nizar because it would provide for different types of memory devices to be compatible with existing systems.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Wednesday, and Thursday from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7467-239 for Official communications, (703) 746-7240 for Non Official communications, and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Denise Tran

12/22/02